Phase Shifts in Single- and Dual-Gate GaAs MESFET's for 2–4-GHz Quadrature Phase Shifters

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Abstract—**The variation of transmission phase for single- and dual-gate GaAs MESFET's with bias change and its probable effects on the performance of an active phase shifter have been studied for the frequency range 2 to 4 GHz. From measured S-parameter values for single- and dual-gate transistors, the element values of the equivalent circuits were fitted by using the computer-aided design program SUPER COMPACT.**

For the normal full-gate voltage range 0 to -2 V at $V_{DS} = 4$ V, the single-gate MESFET varies in transmission phase from 142° to 149° at 2 GHz, and from 109° to 119° at 4 GHz. However, with drain voltage varied from 0.3 to 4 V and a constant gate-voltage bias of 0 V, the phase shifts are much larger, 105° to 145° at 2 GHz and 78° to 112° at 4 GHz. This suggests that large phase shifts may be expected in a dual-gate device and this is found to be so. With $V_{DS} = 4$ V and $V_{GS1} = -1.0$ V, variation of control (second) gate bias from 0 to -1.75 V for the NE463 GaAs MESFET produces a transmission phase variation from 95° to 132° at 2 GHz and 41° to 88° at 4 GHz.

Such phase shifts cause both amplitude and phase errors in phase-shifter circuits of the kind where signals from two FET channels are combined in quadrature with their gate voltages controlled to provide 0° to 90° phase control with constant amplitude. For the single-gate FET examined, the expected amplitude and phase errors are 0.30 dB and 6° at 2 GHz, and 0.36 dB and 10° at 4 GHz. If dual-gate FET's are used in similar circuits, the distribution of errors is different. For NE463 devices, the corresponding figures are 0.56 dB and 2° at 2 GHz and 1.2 dB and 3° at 4 GHz. The advantage of the dual-gate configuration is that the input impedance conditions are more constant than for the single-gate configuration.

I Introduction

PHASE-SHIFT CIRCUITS are needed in phased-array antennas to steer the radiation direction by varying the phase across the array elements. The type of phase shifters to be used is decided by specific requirements like low VSWR, power-handling capability, insertion loss, switching speed, and bandwidth, together with cost, size, weight, and other mechanical considerations. Switched transmission-line phase shifters using p-i-n diodes and ferrite phase shifters are among the technologies used.

With the rapid development of microwave integrated circuits on semi-insulating GaAs substrates, there has appeared a need to realize a phase shifter which can be easily integrated with the rest of the circuitry using the same technology. The p-i-n and ferrite approaches are not convenient for monolithic integration. In this paper, a phase shifter using dual-gate MESFET's reported recently by Kumar *et al.* [1] will be studied. This phase shifter uses the operating principle shown in Fig. 1. Two signals, 90° out-of-phase, are presented to the two channels, namely, x and y. The output of each channel is controlled by a variable gain amplifier using a dual-gate MESFET. These two signals are then combined by an in-phase combiner to produce a resultant vector, as shown in Fig. 1(b). The vector amplitude as well as the angle of rotation can easily be controlled by adjusting the individual x and y components. In this way, one can achieve a phase shift of 0° to 90° and, with four dual-gate FET's, Kumar *et al.* [1] have shown how one may have a full 0°-to-360° phase shift.

This type of phase-shifting technique is different from that studied by Tsironis and Harrop [2], where the intrinsic circuit elements are changed by changing one of the gate biases, and this in turn changes the transmission phase. They obtained a gain of 4 dB with 120° continuous phase shift at 12 GHz. This is suitable for narrow-band applications. The advantages of a dual-gate MESFET phase shifter are stated in [1], to which may be added the advantage of monolithic integration. Such shifters are limited to a low-power stage and are followed by amplification before the signal is fed to the antenna elements. The phase-shifted amplitude reported in [1] shows a fluctuation of ± 2.5 dB; this kind of amplitude variation would produce unacceptable beam control in a phased-array antenna. One cause for such a variation becomes apparent if one considers the way the phase shift is being carried out. For obtaining a 45° phase shift, both the channels are switched on (i.e., 0.0 V on the control gate); then, keeping one of the channels fixed, the other control gate voltage is ramped linearly from 0 V to pinchoff. This rotates the vector resultant from 45° to 0°, as in Fig. 1(c). With the channel action interchanged, the vector is rotated from 45° to 90°. If we assume each channel has constant transmission phase, the resultant amplitude will vary from $(\sqrt{2}A)$ at 45° to A at 0° (or 90^0), where A is the maximum amplitude in any channel with the control gate bias at 0 V. This will cause a

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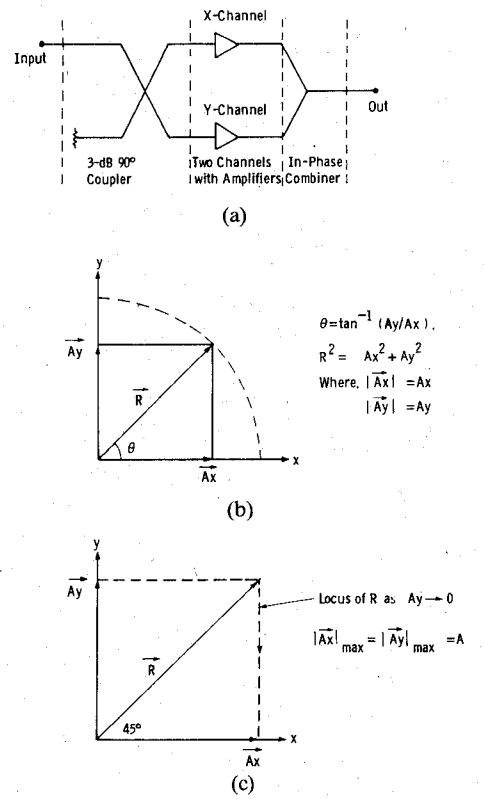

Fig. 1. Quadrature phase shifter operation: (a) Schematic diagram of active phase shifter showing input and output couplers and x- and y-channel amplifiers. (b) Resultant output vector composed of x- and y-channel components. (c) Phase/amplitude pattern used by Kumar *et al.* [1].

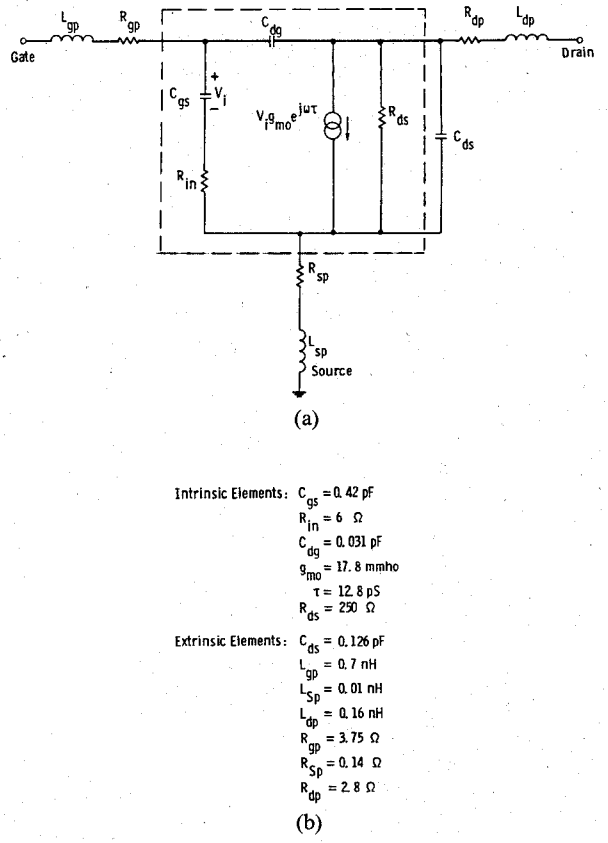

Fig. 2. Equivalent circuit model of the single-gate FET. (a) The circuit model and elements. Intrinsic elements inside the dotted line may change with bias. (b) Typical element values for $V_{DS} = 4.0$ V, $V_{GS} = 0$ V, and $I_{DS} = 34$ mA.

maximum deviation of amplitude at 45°, with respect to the amplitude at phase shifts of 0° and 90°. This accounts for 3-dB variation from the minimum value, occurring at $N \times 90°$ phase shifts, N being an integer. During the subsequent analysis, we will point out that phase variation with gate voltage will add to the amplitude and phase fluctuation.

Before considering phase shifters using dual-gate MESFET's, it is interesting to examine the probable performance of a phase shifter using single-gate FET's in the two channels, instead of dual-gate MESFET's. The gate voltages of the single-gate FET's will be varied to change the amplitudes in the two channels.

Section II describes the variation of the single-gate FET intrinsic elements with gate-bias change and their effect on the transmission phase characteristics. The change in the intrinsic elements with drain-bias change in a single-gate FET and with control gate-bias change in a dual-gate FET are discussed with their effects on the transmission phase in Section III. Section IV shows the overall effects on the performance of single- and dual-gate FET phase shifters and discusses a possible correction for the amplitude error.

While variable gain amplifier-shifters using single- or dual-gate FET's must include matching networks, it is believed that the variation of transmission phase with bias in the FET itself is the primary source of phase errors. This study, therefore, focusses on the FET intrinsic phase response.

II. Transmission Phase Characteristics in a Single-Gate FET

A single-gate GaAs MESFET (LN1-5 #2B) fabricated at Westinghouse was chosen for this investigation. The gate length was 1 μm and the gate width was 4×75 μm. The source–gate distance was 1 μm and the gate–drain distance was 1 μm. The channel doping was $1.1 \times 10^{17}\,\mathrm{cm}^{-3}$ and the pinchoff voltage was just under -2 V on the gate. The S-parameters of this transistor were measured from 2 to 4 GHz at different gate-bias points with the drain voltage fixed. They were then used to determine the equivalent circuit model of Fig. 2. The typical element values after computer fitting using SUPER COMPACT are given in the caption. The bias-voltage variation affects only the intrinsic elements of the equivalent circuit. The parasitics due to bonding wires were, therefore, removed from the model. The resulting circuit has a transmission phase given by

$$\phi = \tan^{-1}(A) - \tan^{-1}\left(\frac{x}{y}\right) \tag{1}$$

where

$$A = \frac{\omega\tau_2 + \sin\omega\tau}{\cos\omega\tau + \omega^2\tau_1\tau_2}$$

$$x = \omega\left(\tau_3\frac{G_{ds}+G_L}{g_{mo}} + \frac{G_s}{g_{mo}}\frac{G_L+G_{ds}}{G_{ds}}\cdot\tau_1 + \frac{G_s}{g_{mo}}\frac{C_{dg}+C_{ds}}{G_{ds}} - \frac{C_{dg}}{G_{ds}} + \cos\omega\tau\right) - \omega^3\tau_1\tau_2\frac{C_{ds}}{G_{ds}} - \omega^2\tau_1\tau_2\left(\frac{G_L+G_{ds}}{G_{ds}}\right)\sin\omega\tau$$

$$y = G_s\left(\frac{G_L+G_{ds}}{G_{ds}g_{mo}} - \frac{\omega^2}{g_{mo}}(\tau_1)\frac{C_{dg}+C_{ds}}{G_{ds}}\right) - \omega^2\tau_1\tau_2\left(\frac{G_L+G_{ds}}{G_{ds}}\right)\cos\omega\tau - \frac{\omega^2}{g_{mo}}\left(C_{gs}\frac{C_{dg}}{G_{ds}} + C_{ds}\tau_3\right) + \omega\frac{C_{dg}}{G_{ds}}\sin\omega\tau$$

in which

τ = transit time in the gate region,
$\tau_1 = R_{in}C_{gs}$,
$\tau_2 = \dfrac{C_{dg}}{g_{mo}}$,
$\tau_3 = (C_{dg}+C_{gs})/G_{ds}$,
$G_s = \dfrac{1}{R_s}$ and $G_L = 1/R_L$.

In the above equation, we have identified three important time constants τ_1, τ_2, and τ_3, which are dependent on elements that change with bias.

The variations of transmission phase and amplitude with gate bias are given in Fig. 3 for 2, 3, and 4 GHz. The phase variation near maximum amplitude (i.e., near $V_G = 0$ V) increases as the frequency increases. In a quadrature phase-shift circuit, this will effectively increase the amplitude variation of the resultant vector tip. A figure of merit can be defined as the ratio of the slope of the magnitude of S_{21} versus gate bias to the slope of the phase of S_{21} with gate bias, i.e.,

$$\text{Figure of merit} = \frac{(|\Delta S_{21}|/\Delta V_G)}{(\Delta < S_{21}/\Delta V_G)}.$$

The higher the figure of merit is, the less the amplitude fluctuations with phase change, as will be seen from the discussion in Section IV. The variation of the FET elements with the gate bias is shown in Fig. 4. As the FET approaches pinchoff, the depletion region under the gate increases. This results in a decrease in both R_{in} and C_{gs}, as shown in the upper curves of Fig. 4. The transit time τ in the gate region also follows the same pattern.

As shown by Engelmann and Liechti [3], the pinchoff of the channel reduces the dipole region. We believe this reduction of charge in the dipole modifies the electric field and so reduces the transit time. The variation of C_{dg} is small. Others who have considered the bias dependence of the elements for the large-signal case include Willing *et al.* [4] and Tajima *et al.* [5]. In our analysis, we have approximately maintained $R_{in}C_{gs}$ proportional to transit time [6].

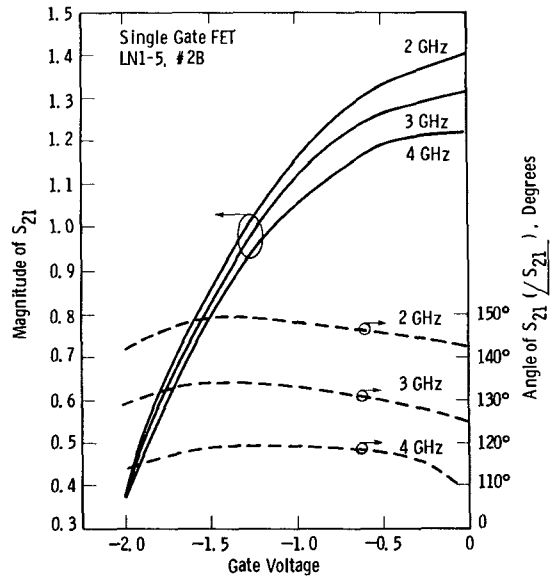

Fig. 3. Amplitude and angle of S_{21} are shown against the gate voltage at 2, 3, and 4 GHz. The values are calculated from the equivalent circuit derived from the measured S-parameters.

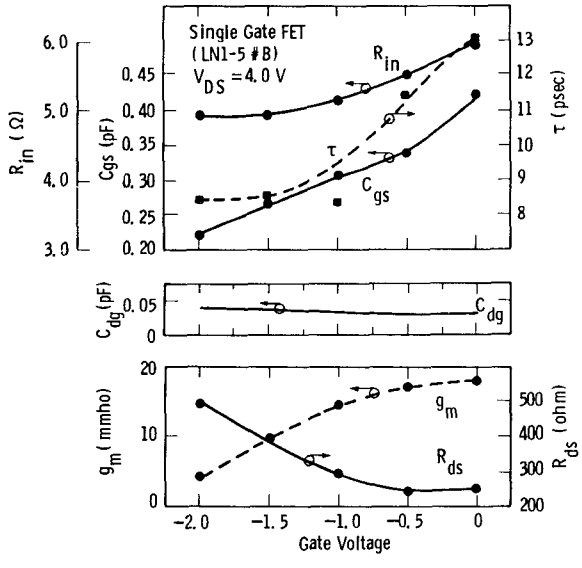

Fig. 4. The variation of the elements in the equivalent circuit of a single-gate FET with change in gate-to-source voltage. The values are obtained through the fitting of the measured S-parameters.

The fall in Fig. 4 of transconductance g_{mo} when approaching pinchoff is expected. The channel resistance R_{ds} shows a small decrease near $V_{GS} = 0$ V and then steadily increases as the channel is pinched off. As these changes occur, the time constants of the device also change.

The effect of each of three previously identified element groups or time constants [$R_{in}C_{gs}$, C_{dg}/g_{mo}, and $(C_{gs}+C_{dg})/G_{ds}$] on the transmission phase of the FET is shown in Table I. These time constants have been varied as the gate-voltage changes. All FET elements were fixed at the $V_{gs} = -1.0$ V values, except those in the time constant being examined. As the time constant was varied, the phase of S_{21} was recorded and the maximum and minimum values at 2 and 4 GHz are noted in Table I. The $R_{in}C_{gs}$

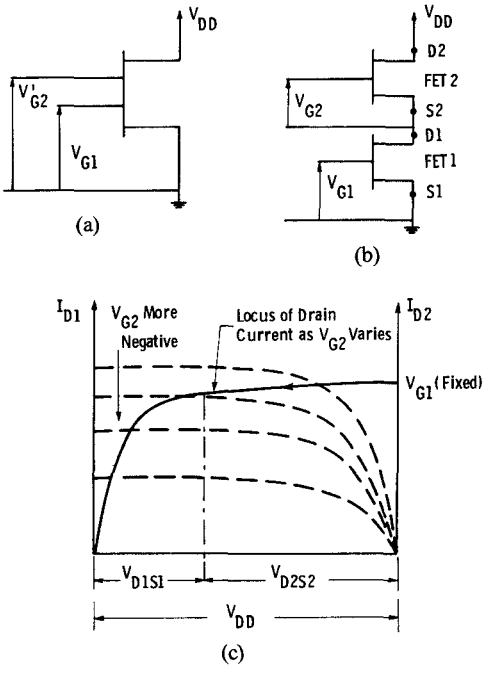

Fig. 5. Dual-gate FET behavior, dc operation. (a) Schematic of dual-gate FET. (b) Equivalent dual-gate FET using two single-gate FET's. FET2 is the load for FET1. (c) For fixed gate voltage on FET1, V_{G1}, the drain current varies as V_{G2} is changed. Operation follows the constant V_{G1} line (solid curve).

TABLE I
CHANGE OF PHASE ANGLE OF S_{21} WITH VARIATION OF CIRCUIT PARAMETERS ASSOCIATED WITH GATE VOLTAGE CHANGE*

FREQ	2 GHz		4 GHz	
$\angle S_{21}$ (deg)	Min	Max	Min	Max
R_{in} and C_{gs} varied	143°	151°	108°	123°
C_{dg}, C_{gs} and G_{ds} varied	143°	149°	111°	119°
C_{dg} and g_{mo} varied	143°	148°	110°	119°

*All the other elements are kept constant at their values for V_{GS} = -1.0 V.

factor produced the greatest impact on the transmission phase, but no single time constant dominated.

The gain of the single-gate FET ($|S_{21}|$) does not change monotonically with gate bias. The gain not only drops off near pinchoff due to a decrease in the transconductance of the device, but it also decreases to a smaller extent near $V_{GS} = 0$ due to the rise in input capacitance C_{gs}. Using the gate voltage of the single-gate FET for gain control, therefore, requires limiting the applied range of gate voltages from pinchoff to less than zero V, if a monotonic gain variation is needed.

III. TRANSMISSION PHASE CHARACTERISTICS OF DUAL-GATE MESFET'S

A dual-gate MESFET can be considered as two single-gate FET's as shown in Fig. 5. Consider the dc operation

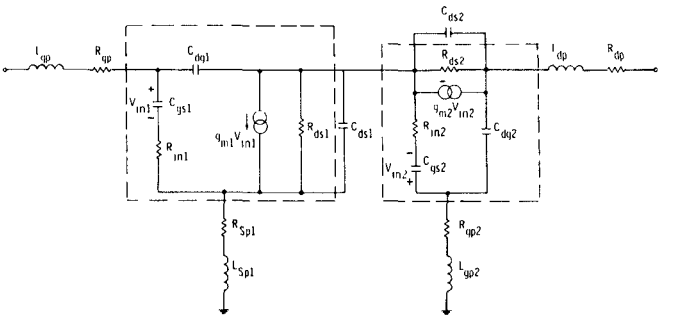

Fig. 6. Equivalent circuit of a dual-gate MESFET used for fitting measured S-parameters. Elements inside the dotted lines are intrinsic and vary with the bias conditions. Typical values are shown in Table II.

TABLE II
EQUIVALENT CIRCUIT ELEMENTS OF A DUAL-GATE MESFET (NE463)

Gate length = 1 μm and width = 2 x 150 μm

Spacing, gate 1 to gate 2 = 3 μm, gate 1 to source = 1 μm

gate 2 to drain = 1 μm

Channel doping $N = 8 \times 10^{16}$ cm^{-3}.

Pinch-off voltage about -2 V

dc Conditions Considered

V_{DD} = 4.0V

V_{G1} = -1.0V

V_{G2} = 0.0V

I_D = 19.9 mA

Intrinsic Components	Extrinsic Components
C_{gs1} = 0.446 pF	L_{glp} = 0.304 nH
R_{in1} = 2.54 ohms	R_{glp} = 3.2 ohms
C_{dg1} = 0.08 pF	R_{sp} = 0.001 ohms
g_{m10} = 29.5 mmho	L_{sp} = 0.001 nH
R_{ds1} = 180 ohms	C_{ds1} = 0.065 pF
τ_1 = 3.76 psec	
C_{gs2} = 0.11 pF	L_{g2p} = 0.001 nH
R_{in2} = 1 ohms	R_{g2p} = 0.001 ohms
C_{dg2} = 0.33 pF	L_{dp} = 0.458 nH
g_{m20} = 29.6 mmho	R_{dp} = 4.31 ohms
R_{ds2} = 240 ohms	C_{ds} = 0.043 pF
τ_2 = 2 psec	

of a dual-gate FET with the voltage at the first gate V_{G1} fixed. The drain current I_{D1} (or I_{D2} since both FET's have the same drain current flowing through them) will be on a particular V_{G1} curve, as shown in Fig. 5(c). The value of I_{d1} will be decided by the load FET2 presents to FET1 and the gate voltage V_{G1}. The total drain voltage will be shared by FET1 and FET2. As V_{G2} is reduced, the drain current will be reduced and the drain voltage on FET1 V_{D1} drops, as shown in Fig. 5(c). FET1 then enters the nonsaturated region. For further negative voltage on V_{G2}, FET2 approaches pinchoff. As FET1 is driven out of saturation, the transconductance of FET1 is reduced.

The microwave equivalent circuit of a dual-gate MESFET is shown in Fig. 6 as a common-source FET connected in series with a common-gate FET. The S-parameters of an NE463 dual-gate GaAs MESFET were measured as a function of the second gate bias V_{G2}. These were used to

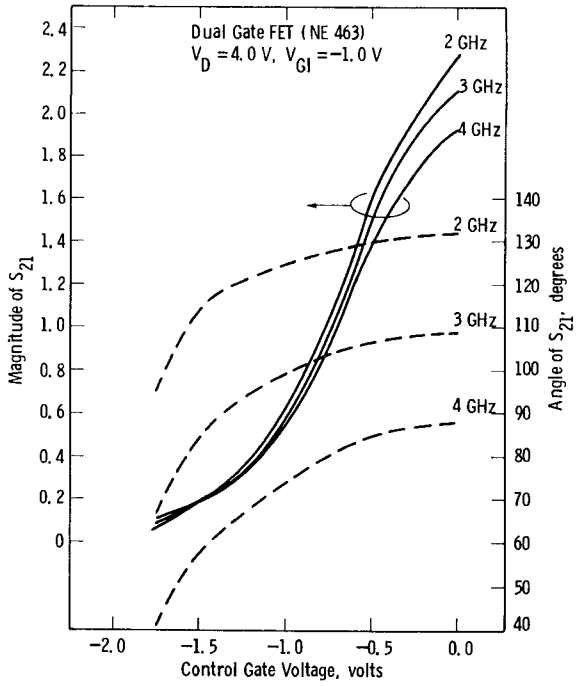

Fig. 7. Amplitude and phase of S_{21} for dual-gate FET versus the control gate voltage.

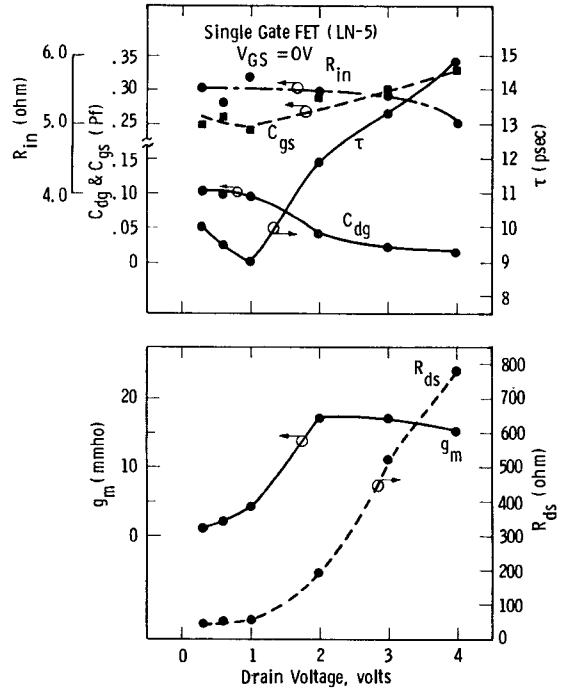

Fig. 8. The variation of the elements in the equivalent circuit of a single-gate FET with change in drain-to-source voltage. The values are obtained through fitting of the measured S-parameters.

derive the values of the equivalent circuit model in Fig. 6. Typical element values are listed in Table II. The parasitics due to bond wires at the source and at the control gate were quite small and were dropped out of the equivalent circuit in the subsequent analysis. The amplitude and phase of S_{21} are plotted against the control gate voltage in Fig. 7. The fall in $|S_{21}|$ is quite steep compared to that in Fig. 3 for the single-gate FET. This implies a rapid fall of g_{m1} as V_{G2}

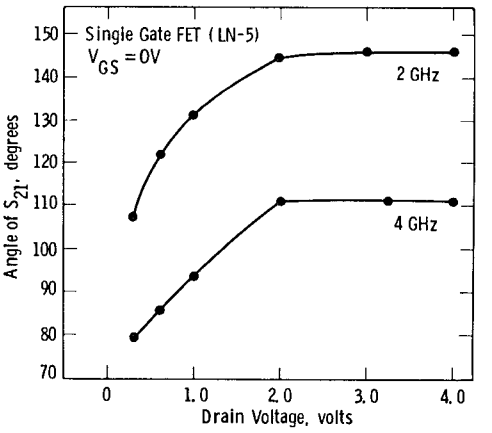

Fig. 9. Transmission phase variation with drain voltage for a single-gate FET. The phase is nearly constant above V_{sat}, but it changes rapidly as the FET goes into nonsaturation.

is made more negative and, hence, control over the gain is achieved.

In order to understand the influence of the particular model elements (or time constants) on phase variation in the dual-gate FET, it is necessary to consider the behavior of FET1 in Fig. 5. This can be represented by a single-gate FET, the drain–source voltage of which is varied and whose gate voltage remains constant.

To review the changes in a single-gate FET as the drain voltage is changed, variations of the circuit elements of a Westinghouse single-gate MESFET with V_{DS} changed from 0.25 to 4.0 V with the gate grounded are shown in Fig. 8. C_{dg} decreases as the drain voltage is increased as expected. The transit time τ first decreases as the drain–source voltage reaches 1 V, then rises substantially, between 1 and 4-V drain bias. The transconductance g_m shows a drop in the nonsaturated region below $V_{DS} = 2$ V. R_{in} is relatively constant over the whole range of drain voltages, while C_{gs} follows the same pattern as reported in [3].

Fig. 9 shows the transmission phase variation of the single-gate FET with the drain voltage. The most important feature is its rapid change in the nonsaturated region below $V_{DS} = 2$ V. The phase of the single-gate FET as a function of gate voltage (Fig. 3) only varied by 10° or less, while Fig. 9 shows over 30° change. The sensitivity of transmission phase with respect to the various time constants described in Section II is shown in Fig. 10. The values of (C_{dg}/g_{mo}) and $C_{dg} + C_{gs}/G_{ds}$ are relatively constant when the FET is saturated at drain voltages above 2 V. Large variations occur below 2 V, however, where C_{dg} rises and g_m falls as the drain voltage approaches zero. The influence of $R_{in}C_{gs}$ is much smaller. With this information as a background, we can now return to consideration of dual-gate FET's.

The variations of the important elements in the equivalent circuit of a dual-gate MESFET (NE463) as the second-gate voltage is changed are shown in Fig. 11. The value of C_{dg} is quite large because of the grounded second-gate pad close to the drain. With an increase of negative bias on the second gate, the drain voltage across FET2 increases and this should reduce C_{dg2}. But, at the same time, FET2 is

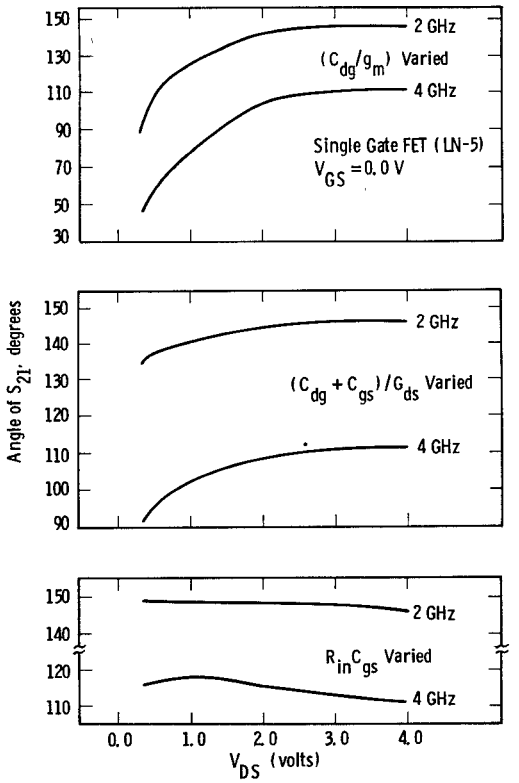

Fig. 10. Variation of transmission phase of single-gate FET time constants; all other elements have been kept fixed at $V_{DS} = 4.0$ V.

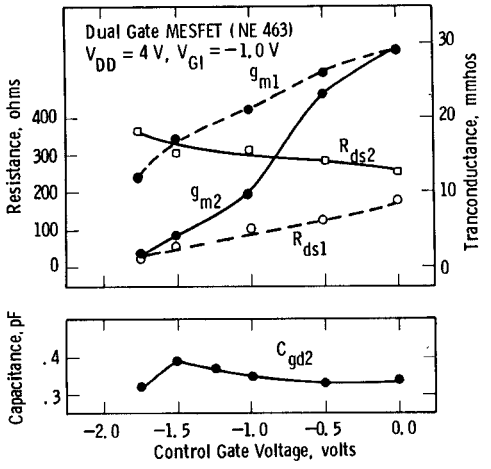

Fig. 11. The variations of selected elements (g_{m1}, g_{m2}, R_{ds}, R_{ds2}, and C_{dg2}) with second-gate voltage. These elements vary the most compared to other elements in the equivalent circuit of the dual-gate FET. The values have been obtained through fitting the measured S-parameters.

tending to pinchoff, which inhibits the formation of any dipole layer near the drain. The lack of dipole formation apparently dominates and keeps C_{dg2} high. The sensitivity of the transmission phase with respect to the transconductances, drain–source resistance, and feedback capacitance is plotted in Fig. 12. It is apparent that altering g_{m1} causes a large variation of transmission phase as a function of second-gate voltage. This is in agreement with the identification of (C_{dg1}/g_{m1}) as the dominant time constant for an FET operated with varying drain voltage on FET1 of the dual-gate FET. Since it is the large variation in g_{m1} with

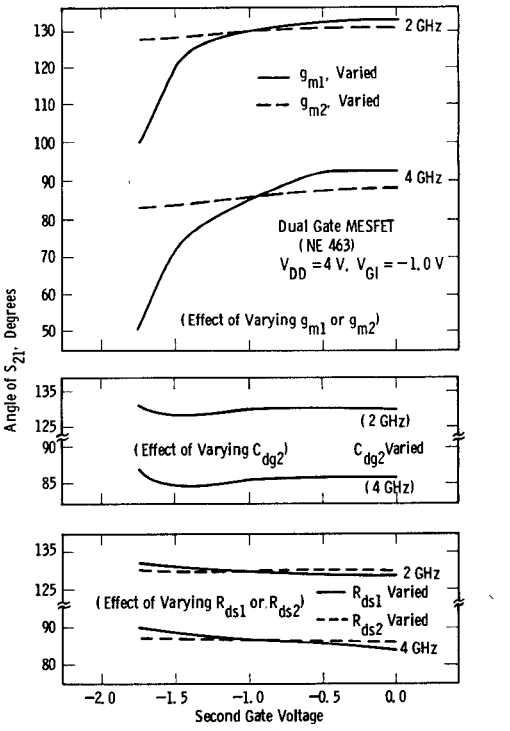

Fig. 12. Transmission phase of a dual-gate FET with respect to different elements in the equivalent circuit. The variable element was assumed to have the values with second-gate bias shown in Fig. 11. All other FET elements are fixed at $V_{G2} = -1.0$ V values.

V_{G2} which enables the dual-gate FET to be used as a gain control element, this implies that no ready solution exists to eliminate the phase variations.

IV. Performance Expected of Phase Shifters Using Single- and Dual-Gate FET's

The performance of a phase shifter employing a quadrature combination of variable amplitude signals, of the type in Fig. 1(a), will now be considered in light of the phase-shift effects discussed in Sections II and III. In Section I, it was pointed out that a part of the amplitude errors displayed in the study by Kumar *et al.* [1] stemmed from the way in which the phase shift was carried out (Fig. 1(c)). A further problem is that the transmission phases of the FET amplifiers change with the bias conditions and therefore the x and y components of the desired vector are only approximately at right angles to each other. Hence, there can be both phase and amplitude errors.

If we combine the outputs, which are 90° apart in phase, of our two single-gate FET's with their gate voltages varied, the maximum phase and amplitude fluctuations for the phase shifter occur at 4 GHz, as shown in Fig. 13. The amplitude reference is taken to be the output of one channel with the other turned off. The transmission phase data are normalized to the phase under these conditions. If only a portion of the total gain variation capability of the single-gate FET is used, where V_G is varied from −0.5 V to pinchoff, the errors at 4 GHz are only ±0.14 dB in amplitude and 4° in phase.

Consider the use of dual-gate MESFET's (NE463) in the phase-shifter circuit. The calculated result for the ampli-

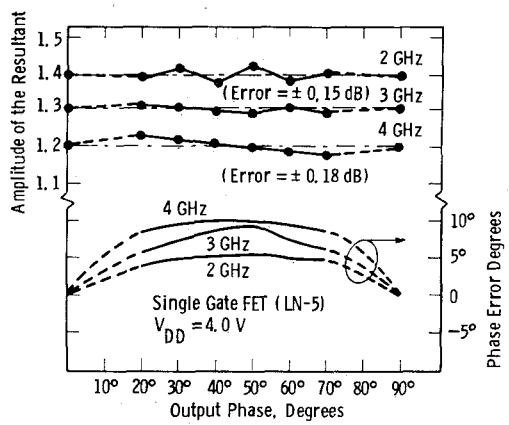

Fig. 13. The calculated vector amplitude and phase variations for the single-gate FET phase shifter. The gate voltage has been varied from 0 V to pinchoff. The dotted portions of the curves have been extrapolated.

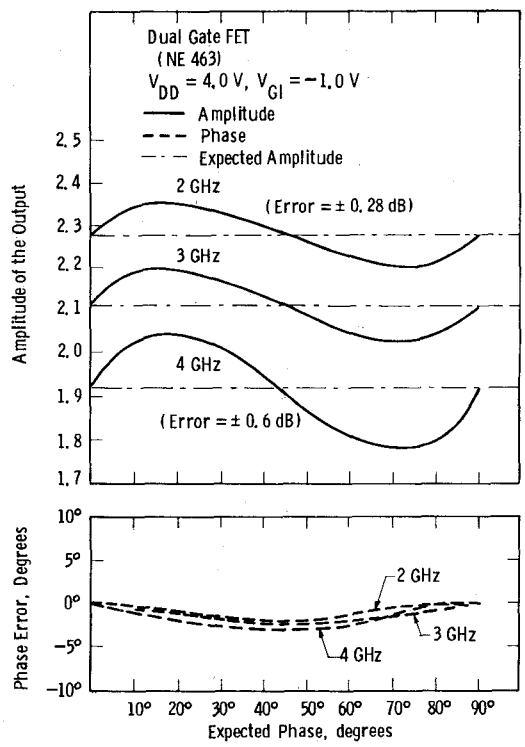

Fig. 14. The calculated vector amplitude (ratio with respect to the input) and phase variations of the dual-gate FET phase shifter. The gate (control) voltage is varied from 0 V to pinch-off.

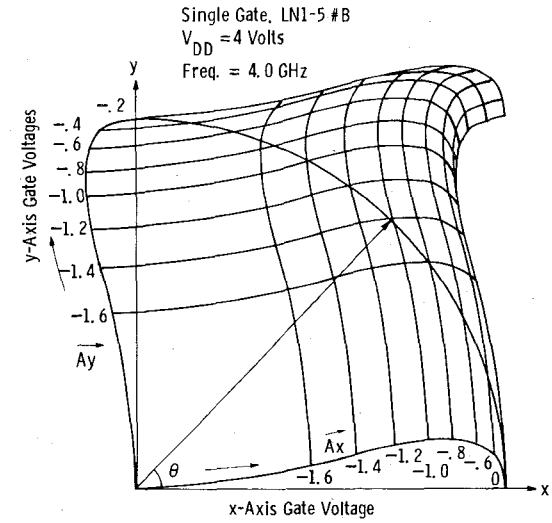

Fig. 15. Polar plot of all possible vectors which can be achieved using a quadrature phase shifter with single-gate FET's. Each grid line represents a 0.2-V step in the gate voltage on the FET. The sample vector lies on an arc from 0 to 90°.

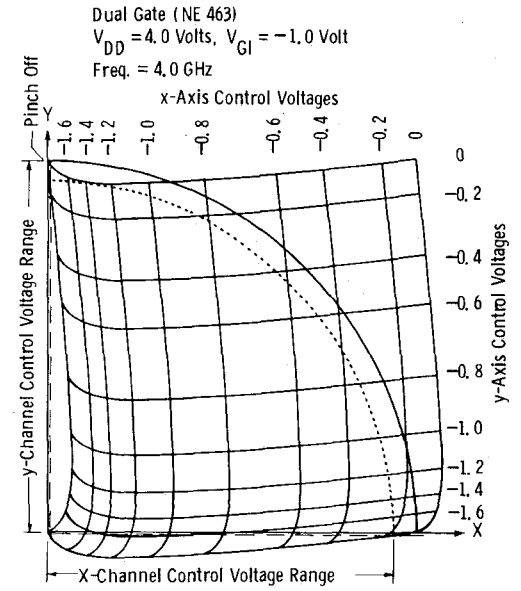

Fig. 16. Polar plot of all possible vectors which can be achieved using a quadrature phase shifter with dual-gate FET's. Each grid line represents a 0.2-V step in control-gate voltage. Since the solid arc lies outside the achievable range near the y axis, the dotted arc must be used with some sacrifice in amplifier gain.

tude and phase errors as a function of the phase shift are shown in Fig. 14. The amplitude error is higher than for the single-gate FET circuit; for instance, ± 0.6 dB at 4 GHz for the dual-gate compared to ± 0.18 dB for the single-gate FET. The maximum phase deviation is only $-3°$ for the dual-gate FET, which is better than for the single-gate FET.

If, in a calibrated phase shifter, a look-up table is provided with appropriate digital values to generate the x- and y-channel biases, it should be possible at any chosen frequency to achieve error-free amplitude at any selected phase. A graphical demonstration of the required bias voltage for entry into such a table is shown in Fig. 15 for the single-gate FET circuit. The loci of A_x and A_y, the components of the desired vector, are drawn at regular intervals of gate voltage parallel to the x and y directions. This gives the total field over which we can produce a vector by some suitable combination of A_x and A_y. As shown in Fig. 15, we can produce the vector at angle θ with a gate voltage of -1.0 V on the x-channel and -1.4 V on the y-channel transistor. Hence, the required table of gate-bias voltages may be readily compiled. The polar plot gives insight into the effects taking place.

A similar chart for the use of dual-gate transistors (NE463) is presented in Fig. 16. The maximum available amplitude represented by the solid lines at 0° and 90°

cannot be maintained, since the locus then swept falls outside the field of the chart when θ exceeds about 80°. Instead, the amplitude of the locus must be reduced to that of the dotted circle that touches the $V_G = 0$ V curve for the y channel. This circle intersects the pinchoff curves for the x and y channels and new quadrature axes x' and y' are drawn through these intersections. Now, the vector rotation must be counted with respect to these new axes. The distance between the two circles is the gain sacrifice to be made to swing the full-phase difference from 0° to 90° with a constant amplitude. In order to obtain this vector, we use the full gate-bias range for the y channel (i.e., 0 to pinchoff), but for the x channel the voltage variation is from slightly below 0 V to pinchoff. This situation will be reversed in the next quadrant, i.e., from 90° to 180° and so on. The presence of input and output matching circuits could be included in such an approach.

This simple graphical representation provides insight into the problem, but it shows only a method of calibration for a single frequency and at a fixed temperature. A family of graphs would be needed to cover a practical wide-band circuit over a usable temperature range, and should include also the effects of input and output matching circuits that are provided.

V. Discussion

The variation of transmission phase and gain with bias change for both single- and dual-gate GaAs FET's has been examined. The ratio of feedback capacitance to transconductance (C_{dg}/g_{mo}) as a function of gate or drain bias dominates the phase variation in these devices. When used in a two-channel, 90° phase shifter, the phase variation in the FET's causes errors in the resultant vector. Considering the magnitude and phase errors in the quadrature phase shifter with both types of FET's, the single-gate device shows better amplitude control over the 0° to 90° range than the dual-gate device.

The choice of which device to use is not determined by only the transmission phase characteristics, however. The single-gate MESFET has no isolation between the input impedance of the device and the control voltage, whereas the dual-gate FET does. This results in a wide variation of C_{gs} as the gate voltage is varied. The input reflection angle of the single-gate device changes as much as 20° when the gate voltage is varied from 0 to −2.0 V at 3 GHz; at 4 GHz, this spread of angle is even greater. The dual-gate device changes its input phase by only 5° as the second-gate bias is reduced from 0 to −1.75 V. Here, the input matching circuits for the circuit with dual-gate transistors may be expected to be easier to design than for a phase shifter with single-gate transistors.

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References

[1] M., Kumar *et al.*, "Broadband active phase shifter using dual gate MESFET," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-29, pp. 1098–1101, Oct. 1981.

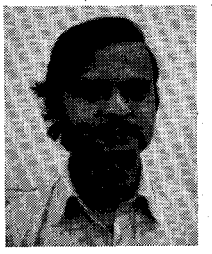
[2] C. Tsironis and P. Hamp, "Dual gate GaAs MESFET phase shifters with gain at 12 GHz," *Electron. Lett.*, no. 14, pp. 553–554, 1980.

[3] R. W. H. Engelmann and C. A. Liechti, "Bias dependence of GaAs and InP MESFET parameters," *IEEE Trans. Electron Devices*, vol. ED-29, no. 11, pp. 1288–1296, Nov. 1977.

[4] H. A. Willing *et al.*, "A technique for predicting large-signal performance of a GaAs MESFET," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-26, pp. 1017–1023, Dec. 1978.

[5] Y. Tajima *et al.*, "GaAs FET large-signal model and its application to circuit designs," *IEEE Trans. Electron Devices*, vol. ED-28, pp. 171–175, Feb. 1981.

[6] H. Statz *et al.*, "Noise characteristic of gallium arsenide field effect transistors," *IEEE Trans. Electron Devices*, vol. ED-21, pp. 549–562, Sept. 1979.



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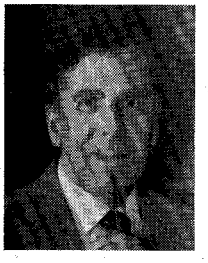

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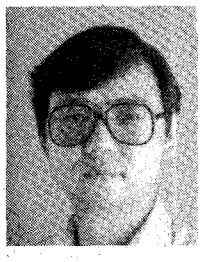

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Correction Due to a Finite Permittivity for a Ring Resonator in Free Space

RONALD DE SMEDT

Abstract—**To better determine the resonant fields of a dielectric resonator with high permittivity ϵ_r, the asymptotic theory with $1/\sqrt{\epsilon_r}$ as a small parameter is extended by adding higher order terms in $1/\sqrt{\epsilon_r}$ in the fields, the resonant wavenumber, and radiation Q. Extensive data are shown for the ϕ-independent "nonconfined" mode of a ring resonator, which radiates as a magnetic dipole. Some results are added for the "magnetic quadrupole" mode.**

I. Introduction

THE CHARACTERISTICS of a dielectric resonator of high permittivity, an important component of microwave circuits [1]–[2], have been investigated extensively [3]–[12]. A solution for arbitrary ϵ_r requires the solution of the field problem for each ϵ_r encountered in practice. This cumbersome procedure can be avoided by introducing a perturbational approach based on a series expansion in $1/N=1/\sqrt{\epsilon_r}$ [9]–[11]. The leading term in these series gives good results as soon as ϵ_r exceeds, say, 100 [11], [13], [14]. Present resonators, however, are based on materials with ϵ_r of the order of 38, because these materials have better temperature coefficients, lower losses, and are more reproducible. The present paper endeavors to extend the limit of applicability of the perturbational approach by evaluating higher order terms in the series in $1/N$. Numerical data are given for the lowest ϕ-independent "nonconfined" resonant modes of a ring resonator located in free space (Fig. 1). These modes radiate either as a magnetic dipole or a quadrupole. The quadrupole mode satisfies an "electric wall" condition in the $z=0$ plane and, hence, is relevant for a resonator located on a metallic plane [13].

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II. Mathematical Formulation

A. Fields

The ϕ-independent fields with azimuthal $\bar{E}$ of an axially symmetric resonator can be derived from a scalar function $\alpha(r, z)$, according to

$$\begin{cases} \bar{E} = -j\dfrac{k}{N} R_c \alpha \bar{\mu}_\phi \\ \bar{H} = \dfrac{1}{r}\operatorname{grad}(r\alpha)\times\bar{\mu}_\phi \end{cases} \tag{1}$$

k is the wavenumber in the dielectric and $R_c=\sqrt{\mu_0/\epsilon_0}=120\pi$ the free-space impedance. r, ϕ, z are cylindrical coordinates with the z-axis along the symmetry axis of the resonator, a meridian cross section of which appears in Fig. 1. By substituting (1) in Maxwell's equations, we find that

$$\begin{cases} \mathcal{L}\alpha + k^2\alpha = 0, & \text{in } S \\ \mathcal{L}\alpha + \dfrac{k^2}{N^2}\alpha = 0, & \text{in } S' \text{ and } S'' \end{cases} \tag{2}$$

where S is the cross section of the inner volume of the resonator and S' and S'' of the outer volume. The differential operator $\mathcal{L}$ is

$$\mathcal{L}\alpha = \frac{\partial^2\alpha}{\partial r^2} + \frac{1}{r}\frac{\partial\alpha}{\partial r} + \frac{\partial^2\alpha}{\partial z^2} - \frac{1}{r^2}\alpha. \tag{3}$$

The functions α and $\partial\alpha/\partial n$ are continuous on C (the interface between resonator and vacuum), while α is zero on the z-axis and regular at infinity. For a dipole mode, α is symmetric about the $z=0$ plane, while for a quadrupole mode it is antisymmetric. To apply the perturbational

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